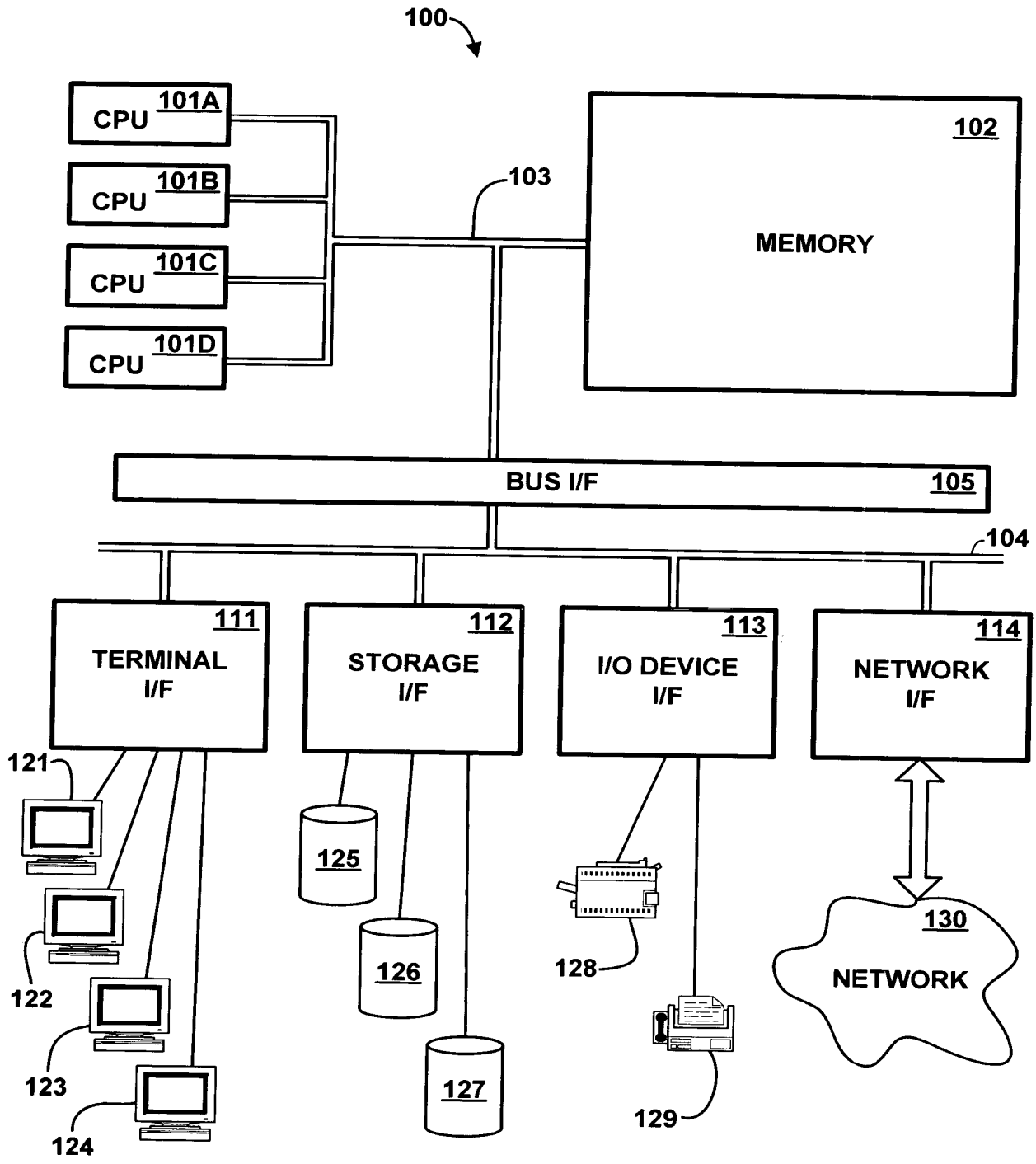
100
CPU 101A
CPU 101B
CPU 101C
CPU 101D
103
102
MEMORY
BUS I/F 105
104
111
TERMINAL I/F
112
STORAGE I/F
113
I/O DEVICE I/F
114
NETWORK I/F
121
122
123
124
125
126
127
128
129
130
NETWORK

FIG.1

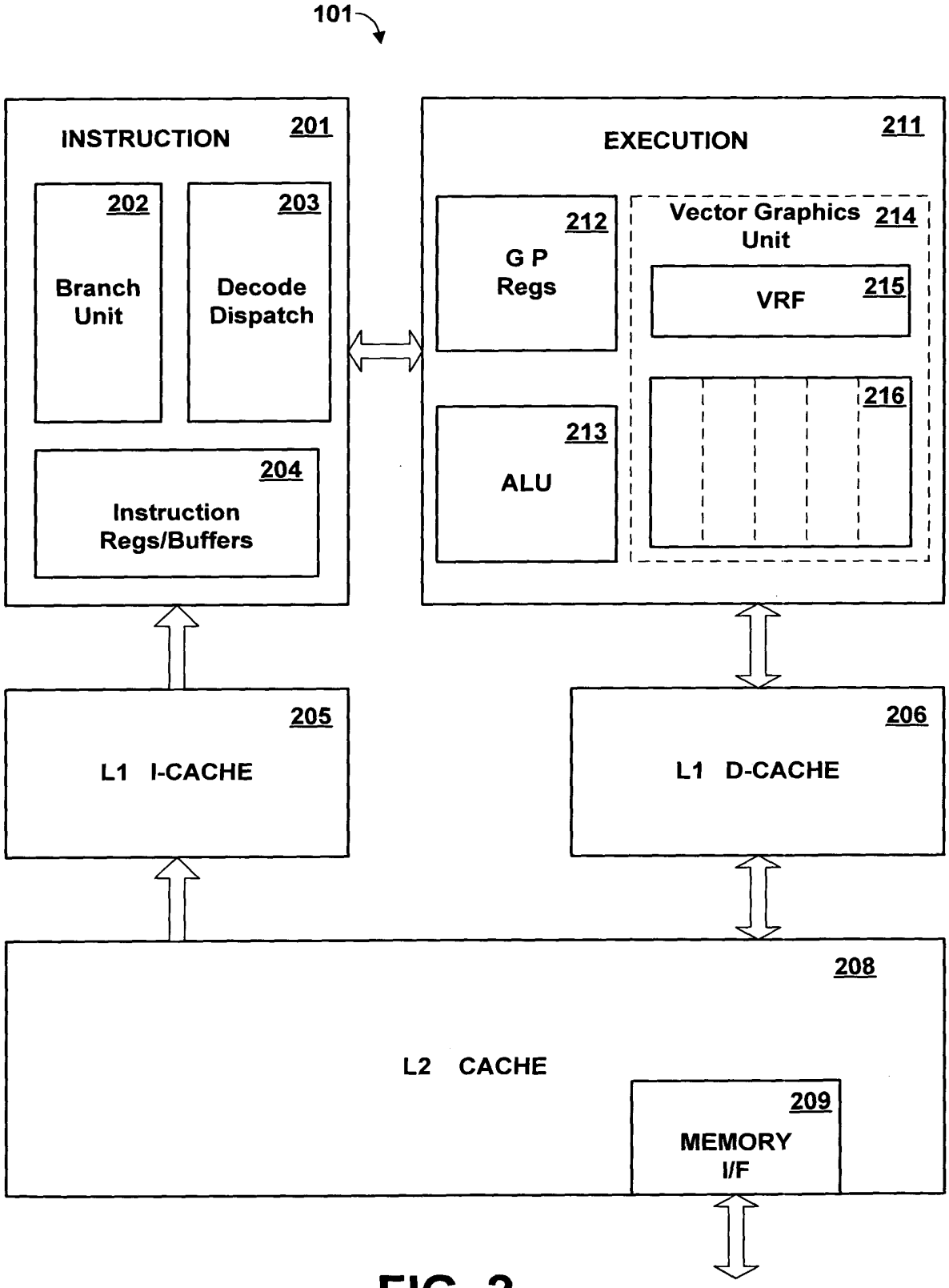
101
INSTRUCTION
201
202
Branch Unit
203
Decode Dispatch
204
Instruction Regs/Buffers
EXECUTION
211
212
G P Regs
Vector Graphics Unit
214
VRF
215
216
213
ALU
205
L1 I-CACHE
206
L1 D-CACHE
208
L2 CACHE
209
MEMORY I/F

FIG. 2

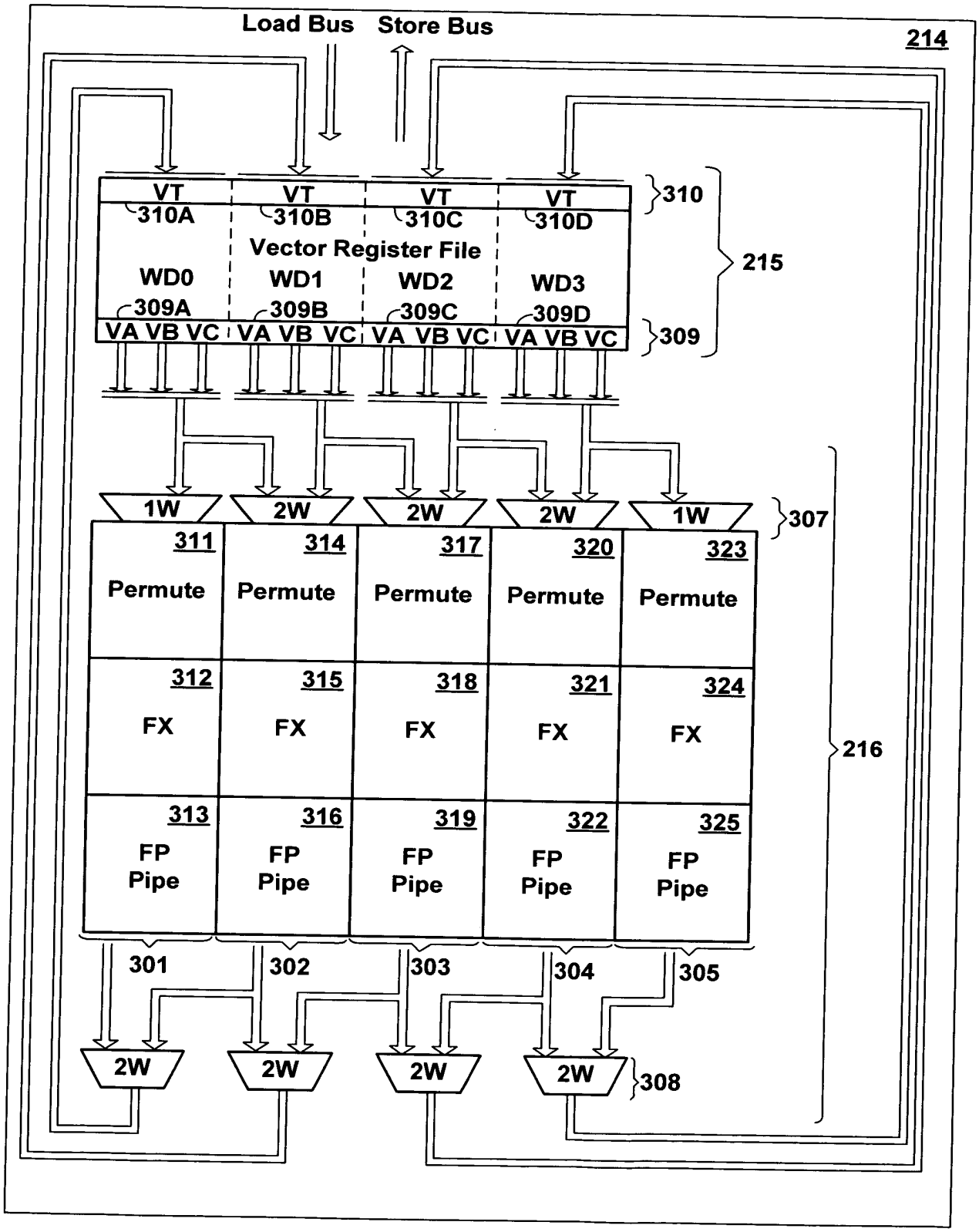
Load Bus
Store Bus
214
VT
310A
VT
310B
VT
310C
VT
310D
310
Vector Register File
215
WD0
309A
WD1
309B
WD2
309C
WD3
309D
VA VB VC
VA VB VC
VA VB VC
VA VB VC
309
1W
2W
2W
2W
1W
307
311
Permute
314
Permute
317
Permute
320
Permute
323
Permute
312
FX
315
FX
318
FX
321
FX
324
FX
216
313
FP Pipe
316
FP Pipe
319
FP Pipe
322
FP Pipe
325
FP Pipe
301
302
303
304
305
2W
2W
2W
2W
308

FIG. 3

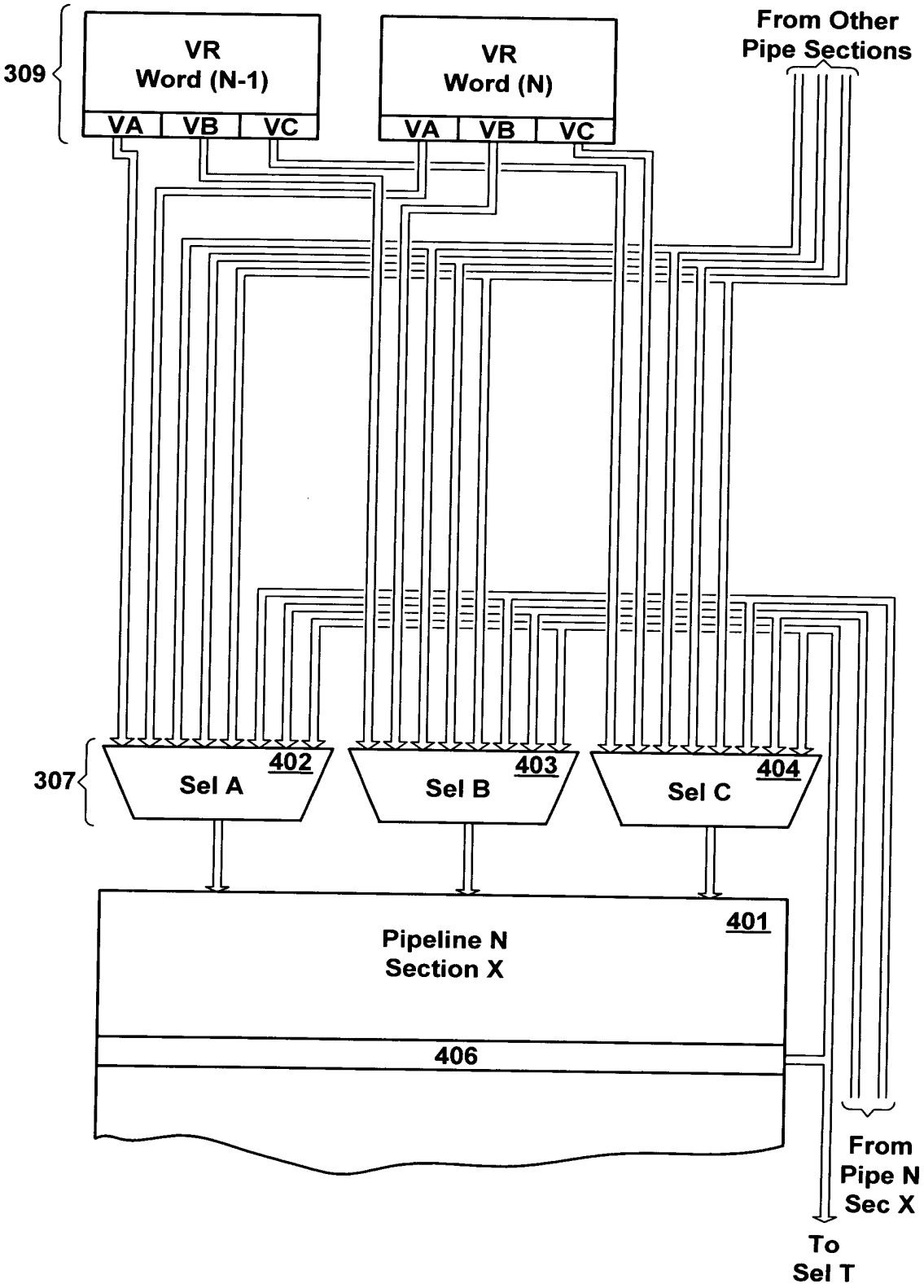
309
VR
Word (N-1)
VA
VB
VC
VR
Word (N)
VA
VB
VC
From Other
Pipe Sections
307
Sel A
402
Sel B
403
Sel C
404
401
Pipeline N
Section X
406
From
Pipe N
Sec X
To
Sel T

FIG. 4A

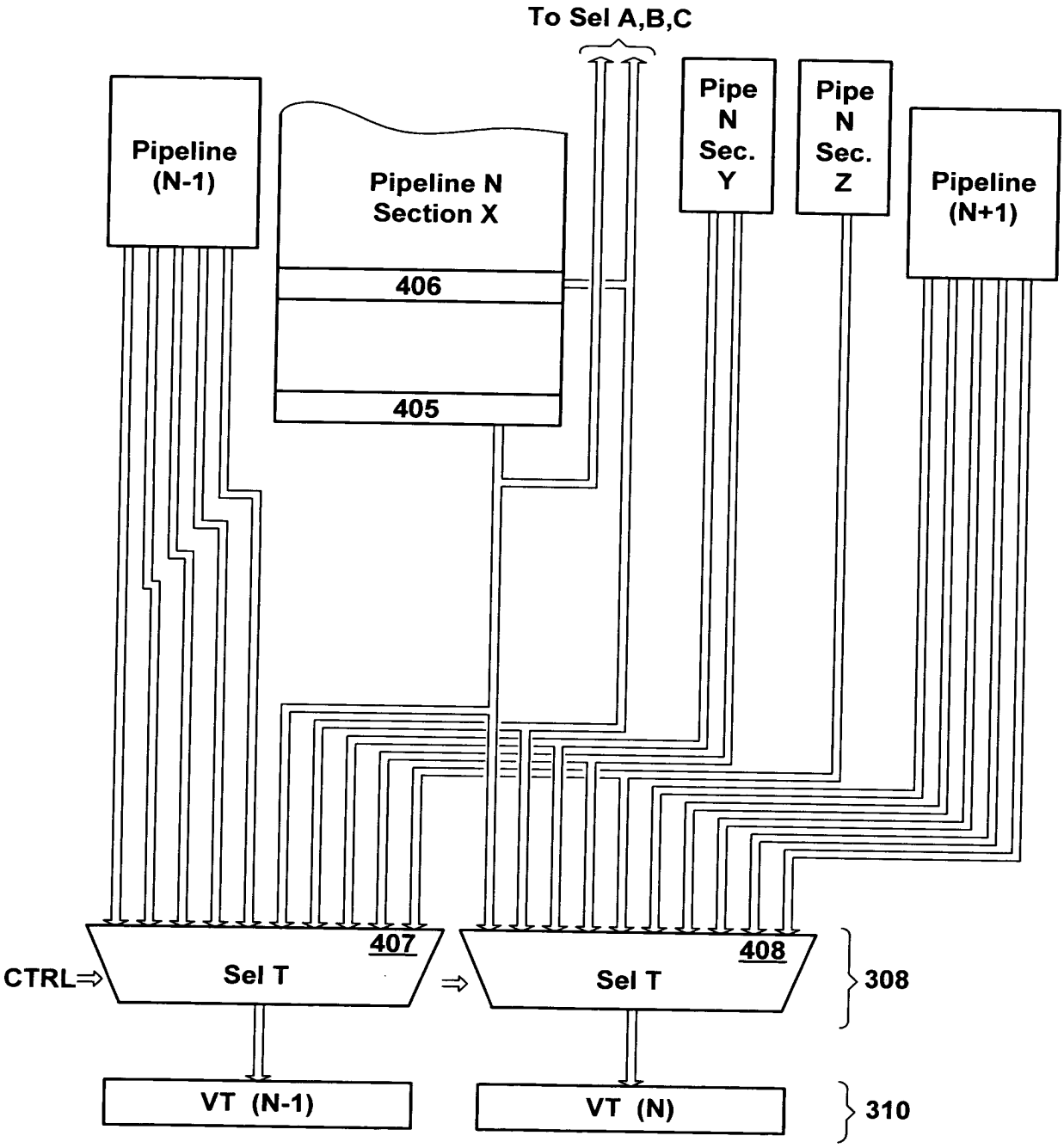
To Sel A,B,C
Pipeline (N-1)
Pipeline N Section X
406
405
Pipe N Sec. Y
Pipe N Sec. Z
Pipeline (N+1)
CTRL⇒
407
Sel T
⇒
408
Sel T
308
VT (N-1)
VT (N)
310

FIG. 4B

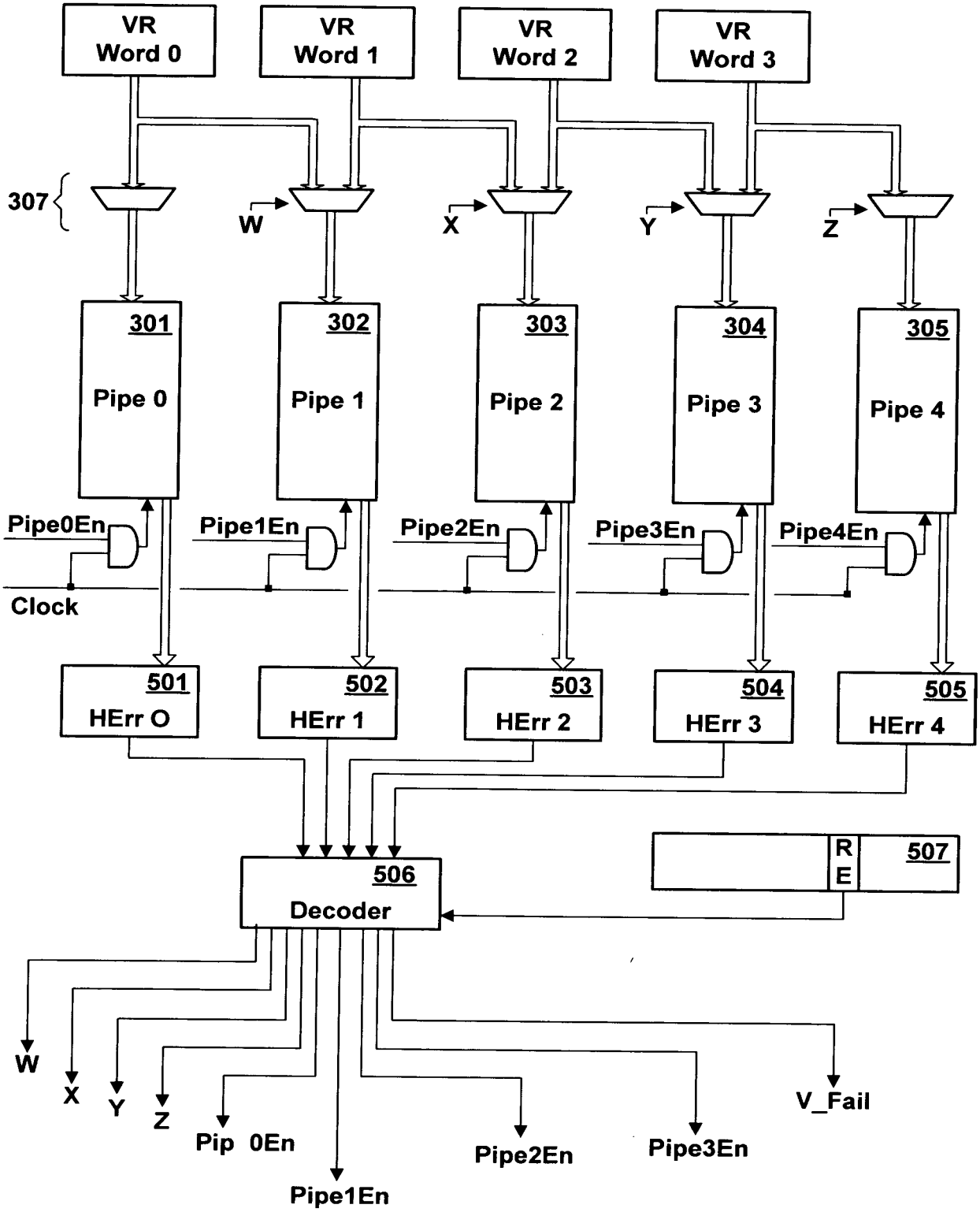
VR Word 0
VR Word 1
VR Word 2
VR Word 3
307
W
X
Y
Z
301
Pipe 0
302
Pipe 1
303
Pipe 2
304
Pipe 3
305
Pipe 4
Pipe0En
Pipe1En
Pipe2En
Pipe3En
Pipe4En
Clock
501
HErr O
502
HErr 1
503
HErr 2
504
HErr 3
505
HErr 4
506
Decoder
RE
507
W
X
Y
Z
Pip 0En
Pipe1En
Pipe2En
Pipe3En
V_Fail

FIG. 5

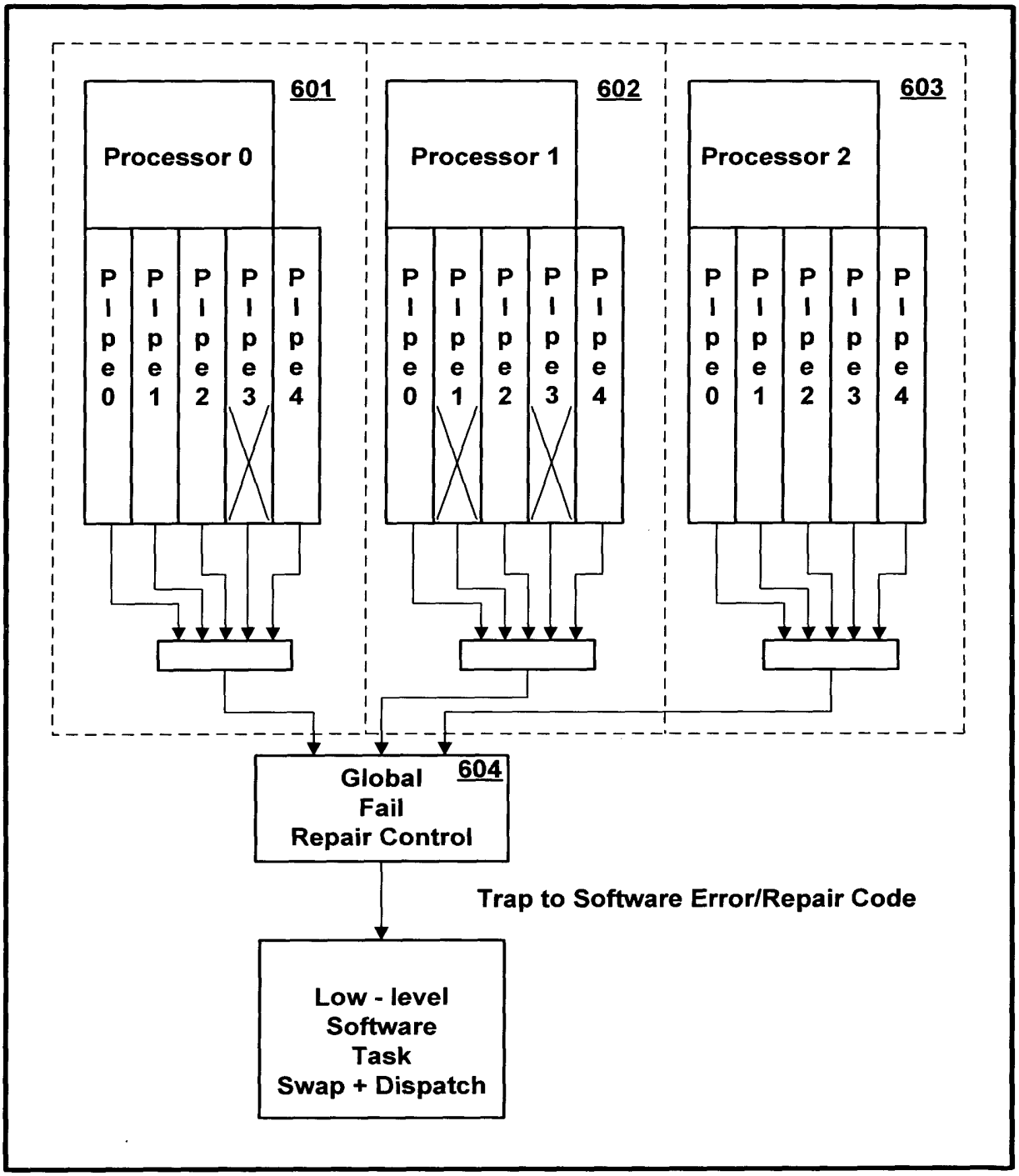
601
Processor 0
602
Processor 1
603
Processor 2
Pipe 0
Pipe 1
Pipe 2
Pipe 3
Pipe 4
Global Fail Repair Control
604
Trap to Software Error/Repair Code
Low - level Software Task Swap + Dispatch

FIG. 6

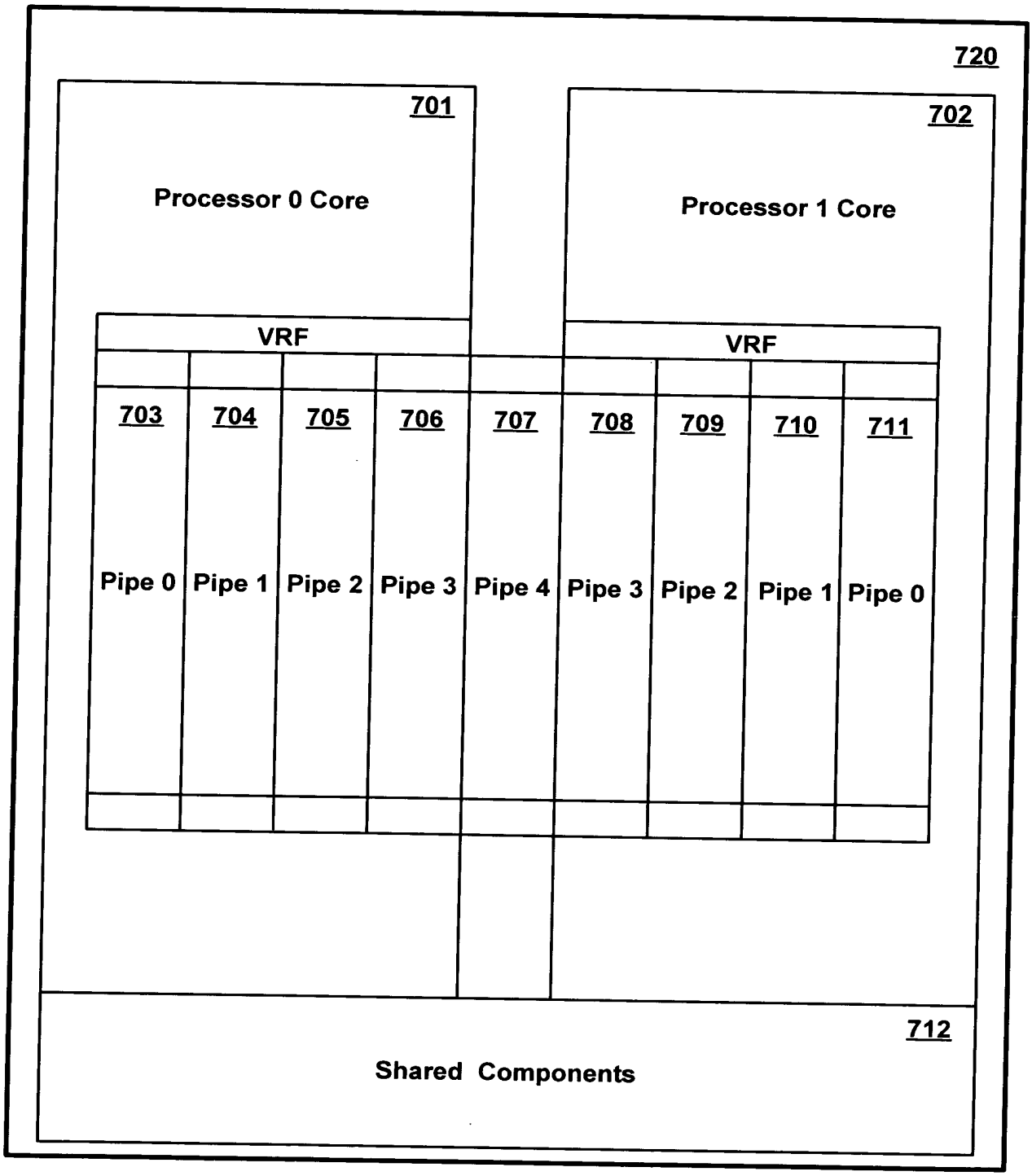
720
701
Processor 0 Core
702
Processor 1 Core
VRF
VRF
703
704
705
706
707
708
709
710
711
Pipe 0
Pipe 1
Pipe 2
Pipe 3
Pipe 4
Pipe 3
Pipe 2
Pipe 1
Pipe 0
712
Shared Components

FIG. 7